

## **Thursday, May 25th: 16:00 – 18:30**

**Opening** 16:00-16:10

Haralampos Stratigopoulos (Sorbonne Université, CNRS, LIP6, France)  
Ioana Vatajelu (Université Grenoble Alpes, Grenoble INP, CNRS, TIMA, France)  
Fei Su (Intel, USA)  
Martin Andraud (Aalto University, Finland)

**Session 1** 16:10-17:00 Keynote

**Today's Manufacturing testing of VLSI chips ain't sufficient — how does that affect AI?**

Rama Govindaraju (Google, USA)

**Session 2** 17:00-18:30

**Securing RISC-V: Challenges and Opportunities**

Jingzhou Li, Huaiyu Chen and Hu He (Tsinghua University, China)

**Computer-Aided Design (CAD) for System-on-Chip Security Validation**

Farimah Farahmandi (University of Florida, USA)

**An Overview on ML Trustworthiness in Adversarial Settings**

Ihsen Alouani (Queen's University Belfast, UK)

**Realizing Federated Learning in Untrusted Environment**

Youssef Allouah, Sadegh Farhadkhani, Rachid Guerraoui, Nirupam Gupta, Rafael Pinot, Geovani Rizk, John Stephan and Sasha Voitovych (EPFL, Switzerland)

**Welcome reception** 19:00

## **Friday, May 26th: 8:30 – 16:00**

**Session 3** 8:30-10:00

**The Impact of Timing Errors in Systolic-Array-Based AI Accelerators**

Stefan Holst, Lim Bumun and Xiaoqing Wen (Kyushu Institute of Technology, Japan)

**Reliability evaluation of Convolutional Neural Network's basic operations on a RISC-V processor**

Fernando Fernandes dos Santos, Angeliki Kritikakou and Olivier Sentieys (University of Rennes, INRIA, IRISA, France)

**A temperature and process compensation circuit for resistive-based in-memory computing array**

Dipesh Monga, Omar Numan, Martin Andraud and Kari Halonen (Aalto University, Finland)

**How does HW AI accelerators based on emerging devices change the way we used to do testing?**

Moritz Fieback, Mottaqiallah Taouil and Said Hamdioui (TU Delft, The Netherlands)

**Coffee Break** 10:00-10:30

**Session 4** 10:30-12:30

**Impact of High-Level-Synthesis on Reliability of Neural Network Hardware Accelerators**

Marcello Traiola, Fernando Fernandes dos Santos, Olivier Sentieys and Angeliki Kritikakou (University of Rennes, INRIA, IRISA, France)

**SNNVerif: A Verification framework for Testing Correctness of Spiking Neural Networks**

Soham Banerjee (International Institute of Information Technology, Pune, India), Sumana Ghosh (Indian Statistical Institute, India), Ansuman Banerjee (Indian Statistical Institute, India) and Swarup Mohalik (Ericsson Research, Bangalore, India)

**Fault Resilience Enhancement of QNNs by Selective TMR enabled by DeepVigor**

Mohammad Hasan Ahmadilivani (Tallinn University of Technology, Estonia), Mahdi Taheri (Tallinn University of Technology, Estonia), Jaan Raik (Tallinn University of Technology, Estonia), Masoud Daneshtalab (Mälardalen University, Sweden), and Maksim Jenihhin (Tallinn University of Technology, Estonia)

**Intelligent diagnosis of unique defects in industrial STT-MRAMs**

Mottaqiallah Taouil, Moritz Fieback and Said Hamdioui (TU Delft, The Netherlands)

**Inexpensive and Unsupervised Screening of Critical Faults using Open-Set Recognition**

Gabriele Gavarini, Annachiara Ruospo, Ernesto Sanchez, Diego Stucchi and Giacomo Boracchi (Politecnico di Torino, Italy)

**Lunch break** 12:30-13:30

**Session 5** 13:30-14:45 Tutorial

**Nervous Systems – From Spiking Neural Networks and Reservoir Computing to Neuromorphic Fault-tolerant Hardware**

Martin A. Trefzer (University of York, UK) and Jim Harkin (Ulster University, UK)

**Session 6** 14:45-15:45

**On the Sensitivity of Analog Artificial Neural Network Models to Process Variations**

Nosheen Afroz (UT Dallas, USA), Ahmad Sayeed Sayem (UT Dallas, USA), Georgios Volanis (UT Dallas, USA), Dzmitry Maliuk (UT Dallas, USA), Haralampos Stratigopoulos (Sorbonne Université, CNRS, LIP6, France) and Yiorgos Makris (UT Dallas, USA)

**An FPGA-Based Hardware Platform for Rapid SNN Prototyping: Demonstration of Test Solutions for Neuromorphic Computing**

Spyridon Raptis, Theofilos Spyrou and Haralampos Stratigopoulos (Sorbonne Université, CNRS, LIP6, France)

**Resilience-Performance Tradeoff Analysis of Deep Neural Network Accelerator**

Salvatore Pappalardo (École Centrale de Lyon, INL, France), Annachiara Ruospo (Politecnico di Torino, Italy), Ian O'Connor (École Centrale de Lyon, INL, France), Bastien Deveautour (CPE Lyon, France), Ernesto Sanchez (Politecnico di Torino, Italy) and Alberto Bosio (École Centrale de Lyon, INL, France)

**Closing** 15:45-16:00

Haralampos Stratigopoulos (Sorbonne Université, CNRS, LIP6, France)  
Ioana Vatajelu (Université Grenoble Alpes, Grenoble INP, CNRS, TIMA, France)  
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